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**AMENDMENTS TO THE CLAIMS:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Previously Presented) An interleaver of a transmitter for interleaving input data bit sequences of  $M$  data bits comprising channel encoded code symbols each consisting of a number  $N$  data bits and control information associated with every code symbol, to be used to control processing in said transmitter and consisting of a number  $L$  of control bits indicating specific states for each corresponding code symbol; comprising:

a0) a channel encoder for receiving digital data in the form of packets from a data source and for encoding said digital data into said channel encoded code symbols of said number  $N$  of data bits;

a) combining means for combining the respective  $N$  data bits of each channel encoded code symbol with the associated  $L$  control bits into a control information/code symbol data word of  $L+N$  bits;

b) control information/code symbol encoding means for encoding said  $L+N$  bit control information/code symbol data words into data words of  $K$  bits, where  $K < L+N$ , according to a predetermined encoding scheme, and

c) an interleaving memory for storing said encoded data words at memory locations thereof.

2. (Previously Presented) An interleaver according to claim 1, further including a write/read means for writing said encoded data words to an interleaving matrix within said interleaving memory at specific memory locations in a row direction and for reading out said encoded data words from said interleaving matrix in the column direction and a control information/code symbol decoding means for decoding said  $K$  bit data words read out from said interleaving matrix in said interleaving memory into said  $N$

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bit code symbols and said L bit control bits according to an inverse of said predetermined coding scheme.

3. (Previously Presented) An interleaver according to claim 1, wherein  $L=4$  and  $N=2$ , wherein said control bits indicate one or more of a frame start, a time slot start, a marker, and a power bit for the code symbol consisting of said 2 data bits.

4. (Previously Presented) An interleaver according to claim 1, wherein one control bit indicates a transmission power ON/OFF control of said code symbols.

5. (Previously Presented) An interleaver according to claim 2, wherein each memory location stores one data word respectively consisting of said encoded combination of a predetermined number N of data bits selected from said input data bit sequence by a selection means of said write/read means and said control bits.

6. (Previously Presented) An interleaver according to claim 1, wherein said channel encoder comprises a convolutional encoder; and said input data bit sequence of M data bits consists of data bit sets each including a predetermined number of bits resulting from a convolutional encoding of a respective data bit using a predetermined coding rate in said convolutional encoder preceding said interleaving memory.

7. (Previously Presented) An interleaver according to claim 1, wherein said interleaving memory has  $N_w \times N_R/K$  memory locations for storing the K data bits of the encoded data words, wherein  $N_w$  denotes the number of columns corresponding to the interleaving depth, K denotes the predetermined number of data bits

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forming one said data word and  $N_R/K$  denotes the number of rows in said interleaving memory.

8. (Previously Presented) An interleaver according to claim 2, wherein said write/read means comprises a selection means for building code symbols by selecting  $N$  respective data bits from  $[n_w + (n-1)N_w + n_r N_w \cdot N]$ -th positions of the input data bit sequence, where  $n = 1, 2, \dots, N$  denotes the  $n$ -th data bit of the code symbol,  $n_w = 0, 1, \dots, N_w - 1$  denotes the column address in the interleaving matrix and  $n_r = 0, 1, \dots, (N_R/K) - 1$  denotes the row address in the interleaving matrix of the data word resulting from a combining encoding of the code symbol and the additional control bite.

9. (Previously Presented) An interleaver according to claim 8, wherein said selection means selects data bits for said code symbols from said input data bit sequence and provides said selected code symbol data bits to said combining means and comprises for  $N=2$  data bits per code symbol and even  $N_w$ :

- two shift register banks each consisting of a first and a second shift register of length  $N_w$ , wherein the even and odd numbered data bits of said input data bit sequence are respectively stored in said first registers of said first and second shift register bank;
- select/write means for selecting at each write cycle 2 data bits of the least significant bit position and the  $N_w/2$  position from the first registers alternately from the first and second register bank and for providing said 2 selected bits as one code symbol to said combining means to be combined with said respective control bits;
- shift means for shifting the register which was read at the last write cycle and the second registers of the register banks while reading in the next odd and even bits of a next input data bit sequence to the respective second register of each register bank; and
- wherein after  $N_w$  alternate data bit selecting and shifting cycles the function of the registers is reversed.

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10. (Previously Presented) An interleaver according to claim 8, wherein said selection means selects data bits for said code symbols from said input data bit sequence and provides said selected code symbol data bits to said combining means and comprises for  $N=2$  data bits per code symbol and odd  $N_w$ :

- two shift register banks each consisting of a first and a second shift register of length  $N_w$ , wherein the even and odd numbered data bits of said input data bit sequence are respectively stored in said first registers (r0) of said first and second shift register bank;

- select/write means for selecting at each write cycle 2 data bits alternately either from the least significant bit position of the first register of the first bank and from the central position  $((N_w-1)/2)$  of the first register of the second bank or from the central position of the first register of the first bank and the least significant bit position of the first register of the second bank, and for writing said 2 selected bits as one code symbol to a respective memory position in said interleaving memory;

- shift means for shifting the two registers which were read at the last write cycle and the registers of the register banks which were not read, while reading in the next odd and even bits of a next input data bit sequence to the respective second register of each register bank; and

- wherein after  $N_w$  alternate data bit selecting and shifting cycles the function of the registers within each bank is reversed.

11. (Previously Presented) A transmitter for transmitting a data bit sequence of  $M$  data bits comprising channel encoded code symbols each consisting of a number  $N$  of data bits together with control information associated with every code symbol, the control information to be used to control processing in said transmitter and consisting of a number  $L$  of control bits indicating specific states for each corresponding code symbol, comprising:

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a0) a channel encoder for receiving digital data in the form of packets from a data source and for encoding said digital data into said channel encoded code symbols of said number N of data bits;

a) combining means for combining the respective N data bits of each channel encoded code symbol with the associated L control bits into a control information/code symbol data word of L+N bits;

b) control information/code symbol encoding means for encoding said L+N control information/code symbol data words into data words of K bits, where  $K < L+N$ , according to a predetermined encoding scheme;

c) processing means for processing said code symbols of said encoded data words in accordance with their control information.

12. (Currently Amended) A transmitter according to claim 11,

said processing means further including a modulation means for modulating said ~~decoded~~ encoded code symbols in accordance to the specific state of the code symbol as indicated by the respective control bits.

13. (Previously Presented) A method for interleaving in a transmitter input data bit sequence of M data bits comprising channel encoded code symbols each consisting of a number N of data bits together with control information (CI) associated with every code symbol, the control information to be used to control processing in said transmitter and consisting of a number L of control bits indicating specific states for each corresponding code symbol, comprising the following steps:

a0) a channel encoder for receiving digital data in the form of packets from a data source and for encoding said digital data into said channel encoded code symbols of said number N of data bits;

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a) combining the respective N data bits of each channel encoded code symbol with the associated L control bits into a control information/code symbol data word of L+N bits;

b) encoding said L+N bit control information/code symbol data words into data words of K bits, where  $K < L+N$ , according to a predetermined encoding scheme; and

c) storing said encoded data words at memory locations of a memory.

14. (Previously Presented) A method according to claim 13, further including the following steps:

writing said encoded data words to an interleaving matrix within said interleaving memory at specific memory locations in a row direction and reading out said encoded data words from said interleaving matrix in the column direction and decoding said K bit data words read out from said interleaving matrix in said interleaving memory into said N bit code symbols and said L bit control bits according to an inverse of said predetermined coding scheme.

15. (Original) A method according to claim 13, further including the following steps:

processing decoded code symbols in accordance to the specific states of the code symbol as indicated by the respective control bits.

16. (Previously Presented) A method according to claim 13 wherein

$L=4$  and  $N=2$ , wherein said control bits indicate one or more of a frame start, a time slot start, a marker, and a power bit for the code symbol consisting of said 2 data bits.

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17. (Previously Presented) A method according to claim 13, wherein one control bit indicates a transmission power ON/OFF control of said code symbols.

18. (Previously Presented) A method for transmitting in a transmitter a data bit sequence of M data bits comprising channel encoded code symbols each consisting of a number N of data bits together with control information associated with every code symbol, the control information to be used to control processing in said transmitter and consisting of a number L of control bits indicating specific states for each corresponding code symbol, comprising the following steps:

a0) a channel encoder for receiving digital data in the form of packets from a data source and for encoding said digital data into said channel encoded code symbols of said number N of data bits;

a) combining the respective N data bits of each channel encoded code symbol with the associated L control bits into a control information/code symbol data word of L+N bits;

b) encoding said L+N control information/code symbol data words into data words of K bits, where  $K < L+N$ , according to a predetermined encoding scheme;

c) processing said code symbols of said encoded data words in accordance with their control information;

d) transmitting said processed code symbols.

19. (Previously Presented) An encoder of a transmitter for transmitting a data bit sequence of M data bits comprising channel encoded code symbols each consisting of a number N of data bits together with control information associated with every code symbol, the control information to be used to control processing in said transmitter and consisting of a number L of control bits indicating specific states for each corresponding code symbol, comprising:

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a0) a channel encoder for receiving digital data in the form of packets from a data source and for encoding said digital data into said channel encoded code symbols of said number  $N$  of data bits;

a) combining means for combining the respective  $N$  data bits of each channel encoded code symbol with the associated  $L$  control bits into a control information/code symbol data word of  $L+N$  bits;

b) control information/code symbol encoding means for encoding said  $L+N$  bit control information/code symbol data words into data words of  $K$  bits, where  $K < L+N$ , according to a predetermined encoding scheme;

c) processing means for processing said code symbols of said encoded data words in accordance with their control information.

20. (Previously Presented) An interleaver of a transmitter for interleaving input data bit sequences of  $M$  data bits comprising channel encoded code symbols each consisting of a number  $N$  of data bits and control information associated with every code symbol, the control information to be used to control processing in said transmitter and consisting of number  $L$  of control bits indicating specific states for each corresponding code symbol comprising:

a0) a channel encoder for receiving digital data in the form of packets from a data source and for encoding said digital data into said channel encoded code symbols of said number  $N$  of data bits;

a) combining means for combining the respective  $N$  data bits of each channel encoded code symbol with the associated  $L$  control bits into a control information/code symbol data word of  $L+N$  bits;

b) control information/code symbol encoding means for encoding said  $L+N$  bit control information/code symbol data words into data words of  $K$  bits, where  $K < L+N$ , according to a predetermined encoding scheme; and



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c) an interleaving memory for storing said encoded data words at memory locations thereof; and

a write/read means for writing said encoded data words to an interleaving matrix within said interleaving memory at specific memory locations in a row direction and for reading out said encoded data words from said interleaving matrix in the column direction and a control information/code symbol decoding means for decoding said K bit data words read out from said interleaving matrix in said interleaving memory into said N bit code symbols and said L bit control bits according to an inverse of said predetermined coding scheme.

21. (Previously Presented) An interleaver of a transmitter for interleaving input data bit sequences of M data bits comprising channel encoded code symbols each consisting of a number N of data bits and control information associated with every code symbol, the control information to be used to control processing in said transmitter and consisting of a number L of control bits indicating specific states for each corresponding code symbol; comprising:

a0) a channel encoder for receiving digital data in the form of packets from a data source and for encoding said digital data into said channel encoded code symbols of said number N of data bits;

a) combining means for combining the respective N data bits of each channel encoded code symbol with the associated L control bits into a control information/code symbol data word of L+N bits;

b) control information/code symbol encoding means for encoding said L+N bit control information/code symbol data words into data words of K bits, where  $K < L+N$ , according to a predetermined encoding scheme; and

c) an interleaving memory for storing said encoded data words at memory locations thereof; and

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a write/read means for writing said encoded data words to an interleaving matrix within said interleaving memory at specific memory locations in a row direction and for reading out said encoded data words from said interleaving matrix in the column direction and a control information/code symbol decoding means for decoding said K bit data words read out from said interleaving matrix in said interleaving memory into said N bit code symbols and said L bit control bits according to an inverse of said predetermined coding scheme, and

each memory location stores one data word respectively consisting of said encoded combination of a predetermined number N of data bits selected from said input data bit sequence by a selection means of said write/read means and said control bits.

22. (Previously Presented) An interleaver of a transmitter for interleaving input data bit sequences of M data bits comprising channel encoded code symbols each consisting of a number N of data bits and control information associated with every code symbol, the control information to be used to control processing in said transmitter and consisting of a number L of control bits indicating specific states for each corresponding code symbol; comprising:

a0) a channel encoder for receiving digital data in the form of packets from a data source and for encoding said digital data into said channel encoded code symbols of said number N of data bits;

a) combining means for combining the respective N data bits of each channel encoded code symbol with the associated L control bits into a control information/code symbol data word of L+N bits,

b) control information/code symbol encoding means for encoding said L+N bit control information/code symbol data words into data words of K bits, where  $K < L+N$ , according to a predetermined encoding scheme; and

c) an interleaving memory for storing said encoded data words at memory locations thereof; and

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a write/read means for writing said encoded data words to an interleaving matrix within said interleaving memory at specific memory locations in a row direction and for reading out said encoded data words from said interleaving matrix in the column direction and a control information/code symbol decoding means for decoding said K bit data words read out from said interleaving matrix in said interleaving memory into said N bit code symbols and said L bit control bits according to an inverse of said predetermined coding scheme, and

said interleaving memory has  $N_w \times N_R/K$  memory locations for storing said the K data bits of the encoded data words, wherein  $N_w$  denotes the number of columns corresponding to the interleaving depth, K denotes the predetermined number of data bits forming one said data word and  $N_R/K$  denotes the number of rows in said interleaving memory; and

said write/read means comprises a selection means for building code symbols by selecting N respective data bits from  $[n_w + (n-1)N_w + n_R N_w N - 1]$ -th positions of the input data bit sequence, where  $n = 1, 2, \dots, N$  denotes the n-th data bit of the code symbol,  $n_w = 0, 1, \dots, N_w - 1$  denotes the column address in the interleaving matrix and  $n_R = 0, 1, \dots, (N_R/K) - 1$  denotes the row address in the interleaving matrix of the data word resulting from a combining encoding of the code symbol and the additional control bits.

23. (Previously Presented) An interleaver of a transmitter for interleaving input data bit sequences of M data bits comprising channel encoded code symbols each consisting of a number N of data bits and control information associated with every code symbol, the control information to be used to control processing in said transmitter and consisting of a number L of control bits indicating specific states for each corresponding code symbol; comprising:

a) combining means for combining the respective N data bits of each channel encoded code symbol with the associated L control bits into a control information/code symbol data word of  $L+N$  bits,

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b) control information/code symbol encoding means for encoding said  $L+N$  bit control information/code symbol data words into data words of  $K$  bits, where  $K < L+N$ , according to a predetermined encoding scheme; and

c) an interleaving memory for storing said encoded data words at memory locations thereof; and

a write/read means for writing said encoded data words to an interleaving matrix within said interleaving memory at specific memory locations in a row direction and for reading out said encoded data words from said interleaving matrix in the column direction and a control information/code symbol decoding means for decoding said  $K$  bit data words read out from said interleaving matrix in said interleaving memory into said  $N$  bit code symbols and said  $L$  bit control bits according to an inverse of said predetermined coding scheme, and

said interleaving memory has  $N_w \times N_R/K$  memory locations for storing said the  $K$  data bits of the encoded data words, wherein  $N_w$  denotes the number of columns corresponding to the interleaving depth,  $K$  denotes the predetermined number of data bits forming one said data word and  $N_R/K$  denotes the number of rows in said interleaving memory; and

said write/read means comprises a selection means for building code symbols by selecting  $N$  respective data bits from  $[n_w + (n-1)N_w + n_R N_w N]$ -th positions of the input data bit sequence, where  $n = 1, 2 \dots N$  denotes the  $n$ -th data bit of the code symbol,  $n_w = 0, 1 \dots N_w - 1$  denotes the column address in the interleaving matrix and  $n_R = 0, 1 \dots (N_R/K) - 1$  denotes the row address in the interleaving matrix of the data word resulting from a combining encoding of the code symbol and the additional control bits; and

said selection means selects data bits for said code symbols from said input data bit sequence and provides said selected code symbol data bits to said combining means and comprises for  $N=2$  data bits per code symbol and even  $N_w$ :

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- two shift register banks each consisting of a first and a second shift register of length  $N_w$ , wherein the even and odd numbered data bits of said input data bit sequence are respectively stored in said first registers of said first and second shift register bank;
- select/write means for selecting at each write cycle 2 data bits of the least significant bit position and the  $N_w/2$  position from the first registers alternately from the first and second register bank and for providing said 2 selected bits as one code symbol to said combining means to be combined with said respective control bits;
- shift means for shifting the register which was read at the last write cycle and the second registers of the register banks while reading in the next odd and even bits of a next input data bit sequence to the respective second register of each register bank; and
- wherein after  $N_w$  alternate data bit selecting and shifting cycles the function of the registers is reversed.

24. (Previously Presented) An interleaver of a transmitter for interleaving input data bit sequences of  $M$  data bits comprising channel encoded code symbols each consisting of a number  $N$  of data bits and control information associated with every code symbol, the control information to be used to control processing in said transmitter and consisting of a number  $L$  of control bits indicating specific states for each corresponding code symbol; comprising:

- a) combining means for combining the respective  $N$  data bits of each channel encoded code symbol with the associated  $L$  control bits into a control information/code symbol data word of  $L+N$  bits,
- b) control information/code symbol encoding means for encoding said  $L+N$  bit control information/code symbol data words into data words of  $K$  bits, where  $K < L+N$ , according to a predetermined encoding scheme; and
- c) an interleaving memory for storing said encoded data words at memory locations thereof; and

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a write/read means for writing said encoded data words to an interleaving matrix within said interleaving memory at specific memory locations in a row direction and for reading out said encoded data words from said interleaving matrix in the column direction and a control information/code symbol decoding means for decoding said K bit data words read out from said interleaving matrix in said interleaving memory into said N bit code symbols and said L bit control bits according to an inverse of said predetermined coding scheme, and

said interleaving memory has  $N_W \times N_R/K$  memory locations for storing said the K data bits of the encoded data words, wherein  $N_W$  denotes the number of columns corresponding to the interleaving depth, K denotes the predetermined number of data bits forming one said data word and  $N_R/K$  denotes the number of rows in said interleaving memory; and

said write/read means comprises a selection means for building code symbols by selecting N respective data bits from  $[n_W + (n-1)N_W + n_R N_W N]$ -th positions of the input data bit sequence, where  $n = 1, 2 \dots N$  denotes the n-th data bit of the code symbol,  $n_W = 0, 1 \dots N_W - 1$  denotes the column address in the interleaving matrix and  $n_R = 0, 1 \dots (N_R/K) - 1$  denotes the row address in the interleaving matrix of the data word resulting from a combining encoding of the code symbol and the additional control bits; and

said selection means selects data bits for said code symbols from said input data bit sequence and provides said selected code symbol data bits to said combining means and comprises for  $N=2$  data bits per code symbol and even  $N_W$ :

- two shift register banks each consisting of a first and a second shift register of length  $N_W$ , wherein the even and odd numbered data bits of said input data bit sequence are respectively stored in said first registers of said first and second shift register bank;
- select/write means for selecting at each write cycle 2 data bits alternatively either from the least significant bit position of the first register of the first bank and from the central position  $((N_W - 1)/2)$  of the first register of the second bank or from the central position of the first register of the first bank and the least significant bit position of the

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first register of the second bank, and for writing said 2 selected bits as one code symbol to a respective memory position in said interleaving memory;

- shift means for shifting the two registers which were read at the last write cycle and the registers of the register banks which were not read, while reading in the next odd and even bits of a next input data bit sequence to the respective second register of each register bank; and

- wherein after  $N_w$  alternate data bit selecting and shifting cycles the function of the registers is reversed.

25. (Previously Presented) An interleaver of a transmitter for interleaving input data bit sequences of  $M$  data bits comprising channel encoded code symbols each consisting of a number  $N$  data bits and control information associated with every code symbol, the control information to be used to control processing in said transmitter and consisting of a number  $L$  of control bits indicating specific states for each corresponding code symbol; comprising:

a channel encoder for receiving digital data in the form of packets from a data source and for encoding said digital data into said channel encoded code symbols of said number  $N$  of data bits

a combiner which combines the respective  $N$  data bits of each channel encoded code symbol with the associated  $L$  control bits into a control information/code symbol data word of  $L+N$  bits;

an encoder which encodes said  $L+N$  bit control information/code symbol data words into data words of  $K$  bits, where  $K < L+N$ , according to a predetermined encoding scheme;

an interleaving memory for storing said encoded data words at memory locations thereof; and

a decoder which derives the control information from the data words;

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a radio frequency transmitter element whose operation is controlled by the control information derived from the decoder.

26. (Previously Presented) An interleaver according to claim 25, further including a write/read means for writing said encoded data words to an interleaving matrix within said interleaving memory at specific memory locations in a row direction and for reading out said encoded data words from said interleaving matrix in the column direction and a control information/code symbol decoding means for decoding said K bit data words read out from said interleaving matrix in said interleaving memory into said N bit code symbols and said L bit control bits according to an inverse of said predetermined coding scheme.

27. (Previously Presented) An interleaver according to claim 25, wherein  $L=4$  and  $N=2$ , wherein said control bits indicate one or more of a frame start, a time slot start, a marker, and a power bit for the code symbol consisting of said 2 data bits.

28. (Previously Presented) An interleaver according to claim 25, wherein one control bit indicates a transmission power ON/OFF control of said code symbols.

29. (Previously Presented) An interleaver according to claim 26, wherein each memory location stores one data word respectively consisting of said encoded combination of a predetermined number N of data bits selected from said input data bit sequence by a selector of said write/read means and said control bits.



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30. (Previously Presented) An interleaver according to claim 25, wherein said input data bit sequence of M data bits consists of data bit sets each including a predetermined number of bits resulting from a convolutional encoding of a respective data bit using a predetermined coding rate in a convolutional encoder preceding said interleaving memory.

31. (Previously Presented) An interleaver according to claim 25, wherein said interleaving memory has  $N_W \times N_R/K$  memory locations for storing the K data bits of the encoded data words, wherein  $N_W$  denotes the number of columns corresponding to the interleaving depth, K denotes the predetermined number of data bits forming one said data word and  $N_R/K$  denotes the number of rows in said interleaving memory.

32. (Previously Presented) An interleaver according to claim 25, wherein the radio frequency transmitter element whose operation is controlled by the control information derived from the decoder is a modulator.

33. (Currently Amended) A radio frequency transmitter comprising:  
a channel encoder for receiving digital data in the form of packets from a data source and for encoding said digital data into said channel encoded code symbols;  
a combiner which combines the channel encoded code symbol with the transmitter control information into a control information/code symbol data word;  
an encoder which encodes the control information/code symbol data word;  
an interleaving memory for storing said encoded data word at memory locations thereof;  
a decoder which derives the control information from the data words;  
a radio frequency transmitter element whose operation is controlled by the control information derived from the decoder,

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wherein the combiner combines respective N data bits of each channel encoded code symbol with associated L control bits into a control information/code symbol data word of L+N bits; and

wherein the encoder, positioned between the combiner and the interleaving memory, encodes the L+N bit control information/code symbol data words into data words of K bits, where  $K < L+N$ .

34. (Previously Presented) An interleaver according to claim 33, wherein the radio frequency transmitter element whose operation is controlled by the control information derived from the decoder is a modulator.

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